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# Astable Oscillator Using the 555 Timer

The $555$ integrated circuit is the most popular chip ever manufactured. Independently produced by more than 10 manufacturers, still in current production, and almost 40 years old, this little circuit has withstood the test of time.

It has been redesigned, improved, and reconfigured in many ways, yet the original design can be bought from many vendors. The design of this chip was right the first time. Originally conceived in 1970 and created by Hans R. Camenzind in 1971, over 1 billion of these ICs were made in 2003 with no apparent reduction in demand. It has been used in everything from toys to spacecraft. Due to its versatility, availability, and low cost it remains a hobbyist favorite.

One of the secrets to its success is it is a true black box, its symbolized schematic is simple and accurate enough that designs using this simplification as a reference tend to work first time. You don’t need to understand every transistor in the base schematic to make it work.

The $555$ Timer IC can be connected either in its Monostable mode to produce a precision timer of a fixed time duration, or in its Bistable mode to produce a flip-flop type switching action. But we can also connect the $555$ timer IC in an Astable mode to produce a very stable $555$ Oscillator circuit for generating highly accurate free running waveforms whose output frequency can be adjusted by means of an externally connected $RC$ tank circuit consisting of just two resistors and a capacitor.

The $555$ in its astable configuration can be used to generate a square wave signal with a number of variations:

• Square wave with even or uneven mark (high) to space (low) ratio

• Pulse train

• Pulse width modulation

• Pulse position modulation

• Frequency modulation

The internal component parts of the $555$ Timer IC together with the IC pin out are illustrated in the adjacent figure, the function of the pins are as follows:

**Pin 1: Gnd = Ground connection.**

**Pin 2:** $\overbar{Trig}$ **= Trigger (active low).**

This active low pin (indicated by the horizontal bar above its name) is normally high (at $+V\_{cc}$) but when it is momentarily taken low (below $1/3 V\_{cc}$) it initiates a sequence of internal events that make the output (pin 3) go high for a period of time set by the value of an external $RC$ time constant.

**Pin 3: Out = Output.**

The output goes high (to $+V\_{cc}$) during a time constant period then returns to 0V. When the IC is operated in astable mode two time constants are involved, one governing the high, and one the low condition. The output is capable of sinking and sourcing up to $200$mA, which makes it capable of driving a number of commonly used devices such as LEDs, relays, lamps and small motors without the need for external driver stages.

**Pin 4:** $\overbar{Res}$ **= Reset (active low).**

Normally high but when taken low makes the $Q$ output of the internal bi-stable to reset to its low state, and $\overbar{Q}$ (the inverse of $Q$) goes to its high state. This immediately makes the output (pin 3) 0V and also causes the Discharge transistor to discharge the external time constant capacitor. If the Reset pin is taken high again the output stays in its reset ($0$V) condition until the IC is triggered once more by an input trigger pulse at pin $2$. In circuits where reset is not required it is normally connected directly to $+V\_{cc}$. The reset pin can also be used as an ‘Inhibit’ control. For example, it can be used to prevent the action of an astable oscillator driving a buzzer, until such time as its signal is needed.

**Pin 5: Ctrl = Control.**

Pin 5 allows for the application of a variable voltage to control the length of time of the $RC$ time constant, and so can be used to vary the frequency and/or the mark to space ratio used in generating the output wave. The higher the voltage on the control pin, the longer the periodic time and the lower the frequency of the astable. This enables the IC to be used for such purposes as frequency modulation, by altering the frequency generated by the $555$ in astable mode in response to a changing voltage or low frequency signal applied to the control pin.

With an astable producing an uneven mark to space ratio (i.e. pulses) the control pin can also be used to vary the mark to space ratio and so produce pulse width modulation (PWM). Alternatively, if the output of the $555$ in astable mode is a series of very narrow negative going pulses, then applying a modulating signal to the control input can be made to vary the high period between the pulses, effectively producing pulse position modulation.

The control pin can also be used with the $555$ in monostable mode to vary the time of the generated delay. When the control pin is not being used for timing control, it is not connected to any external voltage, so to prevent any external noise from entering pin $5$ it is decoupled, typically using a capacitor of around $100$ nF .

As pin $5$ is connected internally to the junction between $R\_{a}$ and $R\_{b}$, the voltage on pin $5$ when not in active use will be $2/3 V\_{cc}$.

**Pin 6: Thresh = Threshold**

In astable mode pin $6$ is connected externally to the $RC$ time constant charging capacitor, and so as the capacitor charges, the voltage on pin $6$ increases. This causes the voltage on the non-inverting input to Comparator $1$, to rise until it reaches the threshold level of $2/3 V\_{cc}$ set by the inverting input of Comparator $1$ being connected to the junction between $R\_{a}$ and $R\_{b}$. Once the voltage on pin $6$ reaches $2/3 V\_{cc}$, Comparator $1$ output suddenly changes state and initiates a sequence of events that causes the external time constant capacitor to begin discharging.

**Pin 7: Disch = Discharge**

Pin $7$ is connected to the collector of the discharge transistor, and once the threshold pin has tripped Comparator $1$ at the end of the charging period for the external timing capacitor, the discharge transistor conducts, causing the discharge period to commence. During this period the output (pin $3$) will be held low until the capacitor has discharged to $1/3 V\_{cc}$ when, in astable mode, the Discharge Transistor will turn off and the charging period will start again. In monostable mode however, the capacitor will be discharged completely to $0$V to await another trigger pulse at pin $2$.

**Pin 8:** $+V\_{cc}$ **= Positive supply voltage**

The $555$ is available in a number of variant forms including BJT and CMOS types. Depending on type they can operate from positive supplies ranging from $0.9$V to $18$V with a current requirement ranging from less than $50$μA to $10$mA for the chip itself. This current requirement must be added to the current needs of any output device, which will be supplied by the output of the $555$ when it is in high mode. This load current can be anything up to $200$mA depending on the load.

**The** $555$ **Astable Oscillator**

As shown to the right, a basic astable requires only two resistors and two capacitors (not including the external load).

The $RC$ time constant that determines the pulse width and frequency is made up of $C\_{1}$, $R\_{1}$ and $R\_{2}$. Pins $6$ and $2$ are connected together, pin $4$ is connected directly to supply as reset is not being used, and the control input on pin $3$ is decoupled with a $C\_{2}=100$ nF capacitor.

To produce a square wave output, with a mark to space ratio approaching $1:1$, $R\_{2}$ should be a much higher value than $R\_{1}$. The reason for this is in the way that the $555$ works.

**Astable operation**

When power is initially applied to pin $8$, capacitor $C\_{1}$ has no charge and so pin $2$, the trigger input is active at $0$V and $C\_{1}$ begins to charge towards the supply voltage ($V\_{cc}$) via $R\_{1}$ and $R\_{2}$. As $C\_{1}$ is also connected to pin $6$, the voltage on the non-inverting (+) input of comparator $1$ also increases. In this condition the output (pin $3$) will be at $V\_{cc}$ and able to act as a source of current to any load, of up to $200$ mA.

The inverting (-) input of comparator $1$ is connected to the resistor chain $R\_{a}$, $R\_{b}$ and $R\_{c}$, which are connected between $V\_{cc}$ and $0$V. Since all three resistors have the same value ($5kΩ$) the voltage on the inverting input will be $2/3 V\_{cc}$.

So long as the voltage on the non-inverting input of comparator $1$ is lower than that on its inverting input, its output will be low (at approximately $0$V), but as soon as $C\_{1}$ charges up to $2/3 V\_{cc}$ the comparator will change to its high level ($V\_{cc}$). This puts a high level on the $R$ (Reset) input of the bistable.

When the $R$ input of the bistable goes high the $Q$ output is reset to zero, and as the $\overbar{Q}$ output is always in the opposite state to the $Q$ output, $\overbar{Q}$ goes high. This has the effect of causing the discharge transistor to conduct heavily, connecting the Discharge pin ($7$) virtually to ground, so discharging the capacitor $C\_{1}$ via $R\_{2}$. The high voltage on the output of the bistable is also fed to the inverter, which changes this level to a ‘low’ of approximately $0$V at the output.

The output of the inverter now allows the output to ‘sink’ up to $200$ mA.

Once the $C\_{1}$ begins to discharge however, the output of comparator $1$ will return to a low level, but this doesn’t matter as the bi-stable will ‘remember’ the very short high pulse delivered to its $R$ input by comparator $1$ and will remain in its ‘reset’ state until it receives a similar ‘set’ pulse at its $S$ input.

Notice that when $C\_{1}$ charged, it did so via both $R\_{1}$ and $R\_{2}$, but it now discharges through $R\_{2}$ only. It is for this reason that $R\_{1}$ is made much smaller than $R\_{2}$. If both resistors were equal in value the discharge time (when the output is low) would be half the charge time (when the output is high). By having a ratio of about $100:1$ for the values of $R\_{2}:R\_{1}$ the mark to space ratio can be made very nearly (but not quite) 1:1.

The falling voltage across $C\_{1}$ is connected to the non-inverting ($+$) input of comparator $2$ so once this voltage falls below that on the inverting ($-$) input, which it will do at a level of $1/3 V\_{cc}$, as the inverting input is fed from the top of the lowest resistor $R\_{c}$ in the potential divider resistance chain, the output of comparator $2$ will go to its high ($V\_{cc}$) level. This is fed to the $S$ input of the bi-stable causing the $Q$ and $\overbar{Q}$ output to swap their high and low states, making the output low once more, switching off the discharge transistor and, via the inverter, making the output (pin $3$) high.

That completes one whole cycle of the output square wave, and $C\_{1}$ now begins to charge once more towards $2/3 V\_{cc}$ and the cycles repeat as long as power is applied.

**Time Constants and the 555**

The relationship between the output wave and the charging and discharging of $C\_{1}$ is illustrated to the right. The charge time is dependent on the time constant $\left(R\_{1}+R\_{2}\right)⋅C\_{1}$ and the discharge time is dependent on the time constant $R\_{2}C\_{1}$ so the discharge time will always be shorter than the charge time. However, when $R\_{2}$ is much greater than $R\_{1}$ the charge and discharge times are nearly equal, and for the purpose of calculating the frequency of oscillation $R\_{1}$ may be ignored, so the period of one cycle is simply the two periods added together.

There is another complication however, the time of the charge or discharge period is not simply the time constant $RC$ because the capacitor is not being allowed to fully charge or discharge, only the central 1/3 of the full charge or discharge is being used, so in calculating the periodic time of the waveform, a constant must be used to modify the normal $τ=RC$ time constant formula.

The figure to the right illustrates how the time constant formula is modified to make it suitable for calculating the periodic times relating specifically to the $555$ astable.

In this example $C\_{1}$ is $50$ nF and it charges via $R\_{1}$ and $R\_{2}$, which have a combined series resistance of $1$MΩ. Therefore the normal time constant ($τ=RC$) is $50$ms and with a supply voltage ($V\_{cc}$) of $10$V, $C\_{1}$ will charge to $3.3$V (1/3Vcc) in $20$ms and reach $6.67$V ($2/3 V\_{cc}$) after $55$ms ($35$ms later).

The voltage across $C\_{1}$ would continue to rise to $10$V after $5$ time constants, except that at $2/3 V\_{cc}$ comparator $1$ will switch on (see above) and $C\_{1}$ will begin its discharge period. $C\_{1}$ has therefore charged for only thirty-five fiftieths ($35/50$) or $0.7$ of the time constant.

**Calculating the Frequency of a 555 Astable**

The output will be high during the charge period when $C\_{1}$ charges via $R\_{1}$ and $R\_{2}$. This is calculated as:

$$τ\_{C}= ln2 \left(R\_{1}+R\_{2}\right)⋅C\_{1}=0.693 \left(R\_{1}+R\_{2}\right)⋅C\_{1}$$

Because $R\_{1}$ does not play a part in the discharge period, the time the output will be low will be given by:

$$τ\_{D}= ln2 R\_{2}C\_{1}=0.693 R\_{2}C\_{1}.$$

The periodic time of the entire wave $(T)$ will therefore be:

$$T=τ\_{C}+τ\_{D}=0.693 \left(R\_{1}+2R\_{2}\right)⋅C\_{1}.$$

As frequency is the inverse of the period, the frequency of a $555$ astable can be written as:

$$f=\frac{1}{T}= \frac{1}{\left(R\_{1}+2R\_{2}\right)⋅C\_{1}}.$$

Finally, the duty cycle of the output will be given by

$$D=\frac{τ\_{c}}{T}=\frac{R\_{1}+R\_{2}}{R\_{1}+2R\_{2}}=\frac{1+ρ}{1+2ρ}$$

where $ρ=R\_{2}/R\_{1}$ is the ratio of the two resistors. So, the duty cycle is determined completely by the relative sizes of the two resistors.

**Design Exercise**

Design an astable multivibrator (free-running oscillator), with $60\%$ duty cycle and frequency equal to the last four digits of your WKU ID ($800$ number). Use a charging capacitor of $0.01$ µF.

## What is the required ratio of the two resistors $R\_{2}:R\_{1}$?

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## Using the last four digits of your WKU ID as the desired frequency, what is the desired period $T$, charging time $τ\_{C}$, and discharging time $τ\_{D}$?

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## What is the required value of the resistor $R\_{2}$?

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## What is the required value of the resistor $R\_{1}$?

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